In the Claims:

1. (*Currently Amended*) Semiconductor device comprising: a substrate with a multilayer structure, the multilayer structure including a quantum well structure having a semiconductor layer sandwiched by further layers of an electrical insulating material, wherein the device is configured as a field effect transistor with a gate, the gate being positioned substantially parallel to the at least one quantum well structure, and the at least one quantum well and ~~the~~ a further quantum well have a distance whereby the at least one quantum well functions as a gate for the further quantum well.

2. (*Previously Presented*) Semiconductor device as claimed in claim 1, characterized in that one or more multilayer substructures each comprising a further semiconductor layer and a further electrical insulator layer are stacked on the quantum well structure forming a superlattice.

3. (*Previously presented*) Semiconductor device as claimed in claim 2, characterized in that the insulator is a high-k material having a larger dielectric constant than that of SiO_2.

4. (*Original*) Semiconductor device as claimed in claim 3, characterized in that the high-k material is crystalline.

5. (*Previously Presented*) Semiconductor device as claimed in claim 4, characterized in that there is epitaxy between the high-k material and the semiconductor material of the semiconductor layer.

6. (*Cancelled*).

7. (*Cancelled*).

8. (*Previously Presented*) Semiconductor device as claimed in claim 1, characterized in that the insulating layer has an equivalent silicon oxide thickness of less than 1 nm.

9. (*Previously Presented*) Semiconductor device-as claimed in claim 1, characterized in that the semiconductor layer comprises silicon.

10. (*Previously Presented*) Semiconductor device as claimed in claim 9, characterized in that the thickness of the semiconductor layer is less than 10 nm.

11. (*Previously Presented*) Semiconductor device, comprising: a substrate with a multilayer structure, the multilayer structure including a quantum well structure having a semiconductor layer sandwiched by further layers of an electrical insulating material, wherein the semiconductor layer is enclosed by high-k materials with different dielectric constants.

12. (*Previously Presented*) Semiconductor device as claimed in claim 1, characterized in that doped regions extending through the quantum well structures form electrical contacts to the quantum well structures.

13. (*Previously Presented*) Semiconductor device as claimed in claim 1, characterized in that there is opposite to the gate a further gate present, which further gate is separated from the gate by the quantum well structures.

Claims 14-22 (*Cancelled*)

23. (*New*) The semiconductor device of claim 11, further including

another quantum well structure separated from said at least one quantum well structure, the at least one quantum well structure functioning as a gate for the other quantum well structure; and

a gate positioned substantially parallel to said at least one quantum well structure to control the semiconductor device as a field-effect transistor.